REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-7 are pending in this application. Claims 10-19 are canceled by the present response without prejudice.

The drawings were objected to for informalities. Claims 3, 11, and 15 were rejected under 35 U.S.C. §112, second paragraph. Claims 10-19 were rejected under 35 U.S.C. §112, second paragraph. Claims 1-19 were rejected under 35 U.S.C. §102(b) as anticipated by JP 09-282237 to Nakano.

Addressing first the objection to the drawings, that objection is traversed by the present response.

The drawings were objected to as the specification at page 15, lines 15-17 referred to the terms "n" and "k", which were shown in the drawings but not clear.

In response to that objection, replacement Figures 4-6 are submitted herein that no longer recite "n" and "k". The drawings instead now recite "if (i = a) j = 0". The specification is also amended to be consistent with such changes in Figures 4-6.

In that respect applicant notes, as indicated in the specification at page 14, line 22, to page 15, line 17, if the value of transfer information "i" is the same as that of an expected value correcting information "a", an error output "j" is fixed at an even number (j = 0). The original specification and drawings indicated "i = 2n" and j = 2k". Those descriptions indicated that only if "i" and "a" are even (i = a = 0), "j" is fixed at an even number (j = 0). However, "j" is fixed at an even number (j = 0) even if "i" and "a" are odd (i = a = 1).

The specification and drawings as noted above are amended to clarify the above aspects that are believed to be clear from the original specification. The presently submitted replacement Figures 4-6 and amendments to the specification at page 15 are believed to address the outstanding objections to the drawings.

Addressing now the rejections of claims 3 and 10-19 under 35 U.S.C. §112, second paragraph, those rejections are traversed by the present response.

Each of claims 10-19 has been canceled by the present response, and thus the rejections thereto are obviated.

Further, claim 3 is amended by the present response to now recite the subject matter noted as omitted therein in the outstanding Office Action at page 3, first paragraph. The amendments to claim 3 are believed to address the rejection thereto under 35 U.S.C. §112, second paragraph.

Addressing now the rejection of claims 1-19 under 35 U.S.C. §102(b) as anticipated by Nakano, that rejection is traversed by the present response.

Independent claim 1 is amended by the present response to clarify features recited therein, and to specifically further recite "an internal circuit which operates based on information held in the information holding circuit". Independent claim 1 now also clarifies the detecting circuit checks the destruction of information held in the information holding circuit "when the internal circuit operates".

Such subject matter clarified in independent claim 1 clarifies a timing in detecting an error in the claimed invention. In the claims as currently written, when an internal circuit operates based on information held in an information holding circuit, a detecting circuit checks destruction of the information. As a non-limiting example such a claimed "internal circuit" can be a memory circuit that is to operate in the semiconductor integrated circuit device of the claims.

Thereby, according to such features clarified in the claims, the claimed device can detect an error (for example destruction of information) that occurs incidentally at any time when an internal circuit (for example a memory circuit) operates.

The claimed features are believed to differ from Nakano.

First, applicant notes the grounds for the outstanding rejection do not clearly indicate how Nakano is applied against the claims. Each grounds for the rejection merely cites the Abstract in Nakano, which is the only part in English, but does not indicate what specific elements in Nakano are corresponded to the claimed features. If any rejection based on Nakano is maintained applicant respectfully requests clarification as how the remote controller 1, EEPROM 2, microcomputer 3, write control part 4a, and read control part 4b in Nakano are being applied against the claims.

Further, applicant respectfully submits the cited disclosure in Nakano is contrary to the claims as currently written. Nakano discloses detecting a data error due to a power source disconnection during data updating and to cope with write incapability. Such an error detection timing in the device of Nakano differs from that in the claims.

More specifically, in Nakano an error can be detected when an internal circuit is put into a non-operating state by shutting off power. This is clear from the "Problem To Be Solved" noted in Nakano that indicates the device therein operates "to cope with a data error due to power source disconnection during data updating". The claims are not directed to detecting an error when a circuit is put into a non-operating state by shutting off power.

In contrast to Nakano, and as clarified in the claims, a detecting circuit can compare an expected value information with compression information of an information compressing circuit to check destruction of information held in the information holding circuit "when the internal circuit operates", "the internal circuit operating based on information held in the information holding circuit". Thereby, in the claims an error can be detected that occurs incidentally when an internal circuit operates, not when an internal circuit is put into a non-operating state as in Nakano.

Applicant respectfully submits Nakano does not disclose or suggest the above-discussed operation or structure in independent claim 1 as currently written. Thereby,

applicant respectfully submits independent claim 1, and the claims dependent therefrom, patentably distinguish over Nakano.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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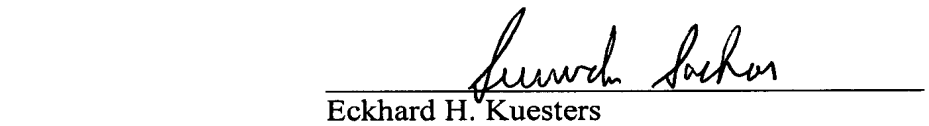

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